Processor config:

1 ADD/SUB F.U. 3 ADD/SUB R.S Units ADD/SUB: 2 cycles0

1 MUL/DIV F.U. 2 MUL/DIV R.S Units MUL: 10 cycles DIV: 40 cycles

Case 1) Normal execution with a couple of RAW dependencies:

|  |  |  |  |
| --- | --- | --- | --- |
|  | Issue | Dispatch | Broadcast |
| I1: DIV F0, F1, F2 | 1 | 2 | 42 |
| I2: ADD F1, F0, F2 | 2 | 43 | 45 |
| I3: ADD F3, F3, F4 | 3 | 4 | 6 |
| I4: SUB F6, F2, F7 | 4 | 7 | 9 |
| I5: MUL F4, F3, F6 | 5 | 42 | 52 |

Case 2) Broadcasting stale result (WAW dependency)

|  |  |  |  |
| --- | --- | --- | --- |
|  | Issue | Dispatch | Broadcast |
| I1: ADD F1, F3, F0 | 1 | 2 | 4 |
| I2: DIV F0, F1, F2 | 2 | 5 | 45 |
| I3: MUL F3, F0, F1 | 3 | 46 | 56 |
| I4: ADD F0, F0, F5 | 4 | 46 | 48 |
| I5: ADD F0, F1, F2 | 5 | 6 | 8 |
| I6: DIV F1, F7, F0 | 46 | 56 | 96 |
|  |  |  |  |

I4 broadcasts stale result

Case 3) RS gets filled, so issue should be stalled:

|  |  |  |  |
| --- | --- | --- | --- |
|  | Issue | Dispatch | Broadcast |
| I1: DIV F0, F1, F2 | 1 | 2 | 42 |
| I2: ADD F1, F0, F2 | 2 | 43 | 45 |
| I3: ADD F3, F3, F4 | 3 | 4 | 6 |
| I4: ADD F2, F3, F4 | 4 | 7 | 9 |
| I5: SUB F6, F2, F7 | 7 | 10 | 12 |
| I6: ADD F4, F5, F7 | 10 | 12 | 14 |

Case 4) Broadcasting in the same cycle:

|  |  |  |  |
| --- | --- | --- | --- |
|  | Issue | Dispatch | Broadcast |
| I1: MUL F0, F0, F1 | 1 | 2 | 12 |
| I2: ADD F1, F1, F2 | 2 | 3 | 5 |
| I3: ADD F2, F1, F2 | 3 | 6 | 8 |
| I4: ADD F3, F4, F3 | 4 | 8 | 10 |
| I5: SUB F4, F4, F5 | 6 | 10 | 12 |